Dual High Frequency Differential Amplifier For Low Power Applications Up to 500MHz

General Description

The **αRD3102** consists of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 1GHz. These features make the **αRD3102** useful from DC to 500MHz. Bias and load resistors have been omitted to provide maximum application flexibility. The monolithic construction of the **αRD3102** provides close electrical and thermal matching of the amplifiers. This feature makes this device particularly useful in dual channel applications where matched performance of the two channels is required.
The **αRD3102** has a separate substrate connection for greater design flexibility.

Features

- **Power Gain 23dB (Typ). 200MHz**
- **Noise Figure 4.6dB (Typ) 200MHz**
- **Two Differential Amplifiers on a Common Substrate**
- **Independently Accessible Inputs and Outputs**
- **Full Military Temperature Range . . . . . -55°C to 125°C**

Applications

- **VHF Amplifiers**
- **VHF Mixers**
- **Multifunction Combinations - RF/Mixer/Oscillator; Converter/IF**
- **IF Amplifiers (Differential and/or Cascode)**
- **Product Detectors**
- **Doubly Balanced Modulators and Demodulators**
- **Balanced Quadrature Detectors**
- **Cascade Limiters**
- **Synchronous Detectors**
- **Balanced Mixers**
- **Synthesizers**
- **Balanced (Push-Pull) Cascode Amplifiers**
- **Sense Amplifiers**

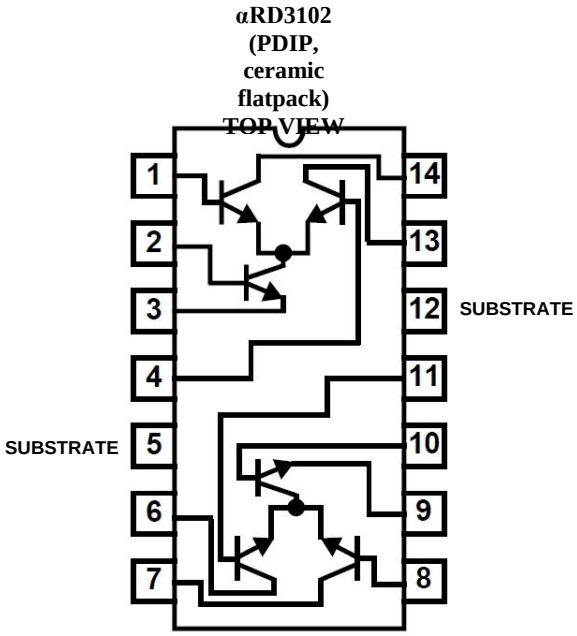
Ordering information

Table 1

Part	Temp. range, °C	Package	Package drawing	Burn-In case temp, °C	Burn-In time, hrs
αRD3102	–55 to +125	14-pin plastic DIP	Figure 6	+125	240
αRD3102	–55 to +125	14-lead ceramic flatpack	Figure 7	+125	240

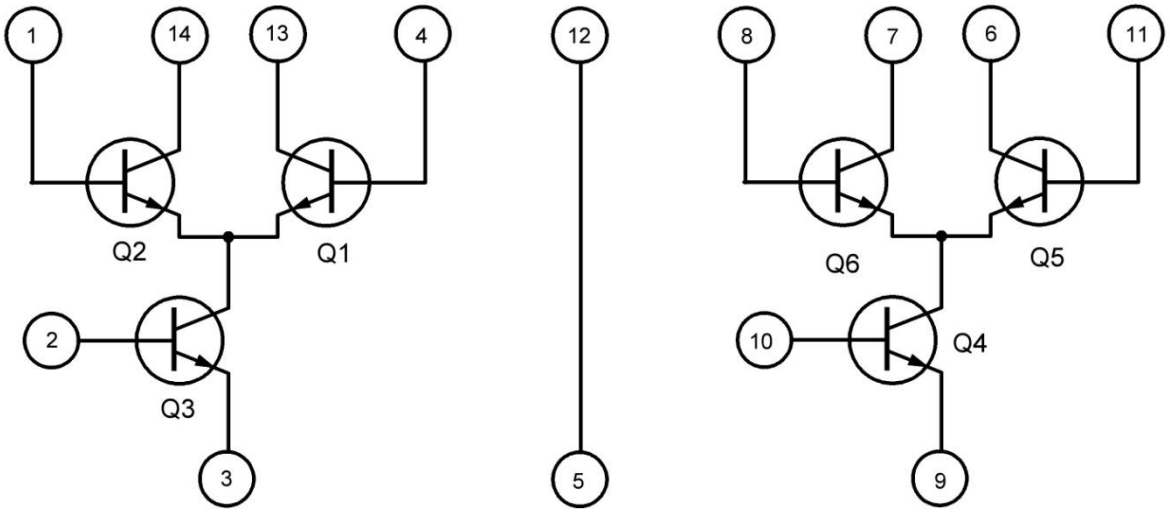
Pinout

Figure 1



Schematic Diagrams

Figure 2



Substrate

Absolute maximum ratings

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) .. 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, IC 50mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 110
Ceramic flatpack Package 205
Maximum Power Dissipation (Any One Transistor) 300mW
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 260°C
(ceramic flatpack - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the **αRD3102** is isolated from the substrate by an integral diode. The substrate (Terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications TA = 25°C

Table 2

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER							
Input Offset Voltage	V_{IO}			-	0.25	5.0	mV
Input Offset Current	I_{IO}	$I_3 = I_9 = 2mA$		-	0.3	3.0	µA
Input Bias Current	I_B			-	13.5	33	µA
Temperature Coefficient Magnitude of Input Offset Voltage	$\lvert\Delta V_{IO}\rvert/\Delta T$			-	1.1	-	µV/°C
DC CHARACTERISTICS FOR EACH TRANSISTOR							
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6V$, $I_C = 1mA$		674	774	874	mV
Temperature Coefficient of Base-to-Emitter Voltage	$\Delta V_{BE}/\Delta T$	$V_{CE} = 6V$, $I_C = 1mA$		-	-0.9	-	mV/°C
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$		-	0.0013	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$		15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10µA$, $I_E = 0$		20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10µA$, $I_B = I_E = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10µA$, $I_C = 0$		5	7	-	V
DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER							
1/f Noise Figure (For Single Transistor)	NF	f = 100kHz, $R_S = 500Ω$, $I_C = 1mA$		-	1.5	-	dB
Gain Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6V$, $I_C = 5mA$		-	1.35	-	GHz
Collector-Base Capacitance	C_{CB}	$I_C = 0$, $V_{CB} = 5V$	Note 3	-	0.28	-	pF
			Note 4	-	0.15	-	pF
Collector-Substrate Capacitance	C_{CI}	$I_C = 0$, $V_{CI} = 5V$		-	1.65	-	pF
Common Mode Rejection Ratio	CMRR	$I_3 = I_9 = 2mA$		-	100	-	dB
AGC Range, One Stage	AGC	Bias Voltage = -6V		-	75	-	dB
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10MHz		-	22	-	dB

Electrical Specifications TA = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Insertion Power Gain	G_P	V_{CC} = 12V, for Cascode Configuration $I_3 = I_9$ = 2mA. For Diff. Amp.Configuration $I_3 = I_9$ = 4mA (Each Collector $I_C \approx$ 2mA) f = 200MHz	Cascode	-	23	-	dB
Noise Figure	N_F		Cascode	-	4.6	-	dB
Input Admittance	Y_{11}		Cascode	-	1.5 + j2.45	-	mS
			Diff. Amp.	-	0.878 + j1.3	-	mS
Reverse Transfer Admittance	Y_{12}		Cascode	-	0.0 - j0.008	-	mS
			Diff. Amp.	-	0.0 - j0.013	-	mS
Forward Transfer Admittance	Y_{21}		Cascode	-	17.9 - j30.7	-	mS
			Diff. Amp.	-	-10.5 + j13	-	mS
Output Admittance	Y_{22}		Cascode	-	-0.503 - j15	-	mS
			Diff. Amp.	-	0.071 + j0.62	-	mS

NOTES:
3. Terminals 1 and 14 or 7 and 8.
4. Terminals 13 and 4 or 6 and 11.

Test Circuits

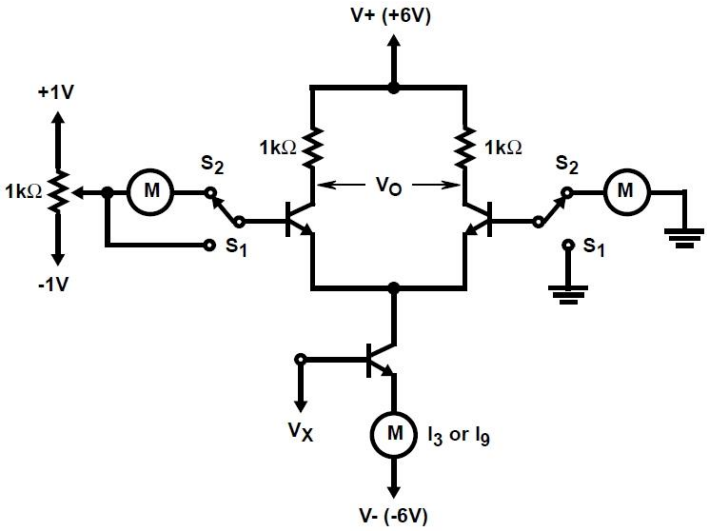


FIGURE 3. DC characteristics test circuit for αRD3102

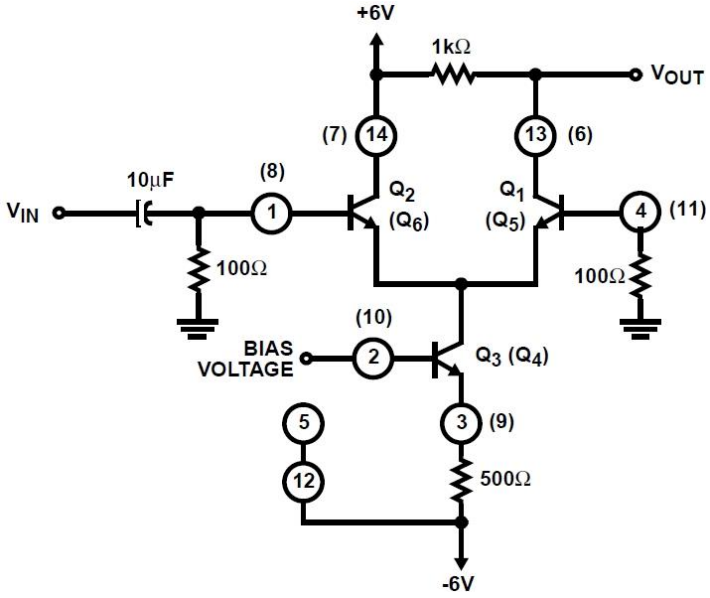
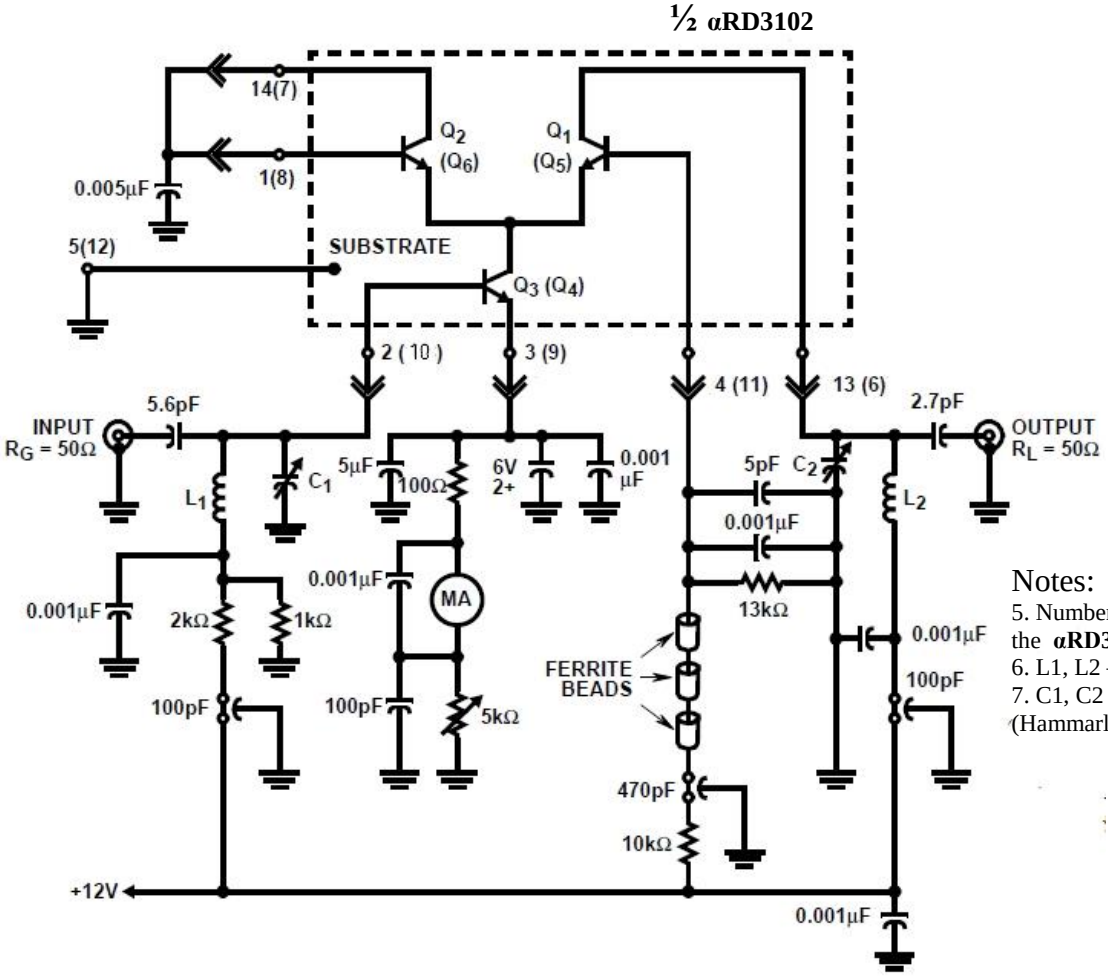


FIGURE 4. AGC range and Voltage Gain test circuit for αRD3102



Notes:

5. Numbers in parentheses refer to other half of the **αRD3102**
6. L1, L2 – Approximately ½ Turn # 18
7. C1, C2 – 15pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent).

FIGURE 5. 200MHz Cascode Power Gain and Noise figure test circuit

Physical Dimensions Figure 6.

14-PIN PLASTIC DIP

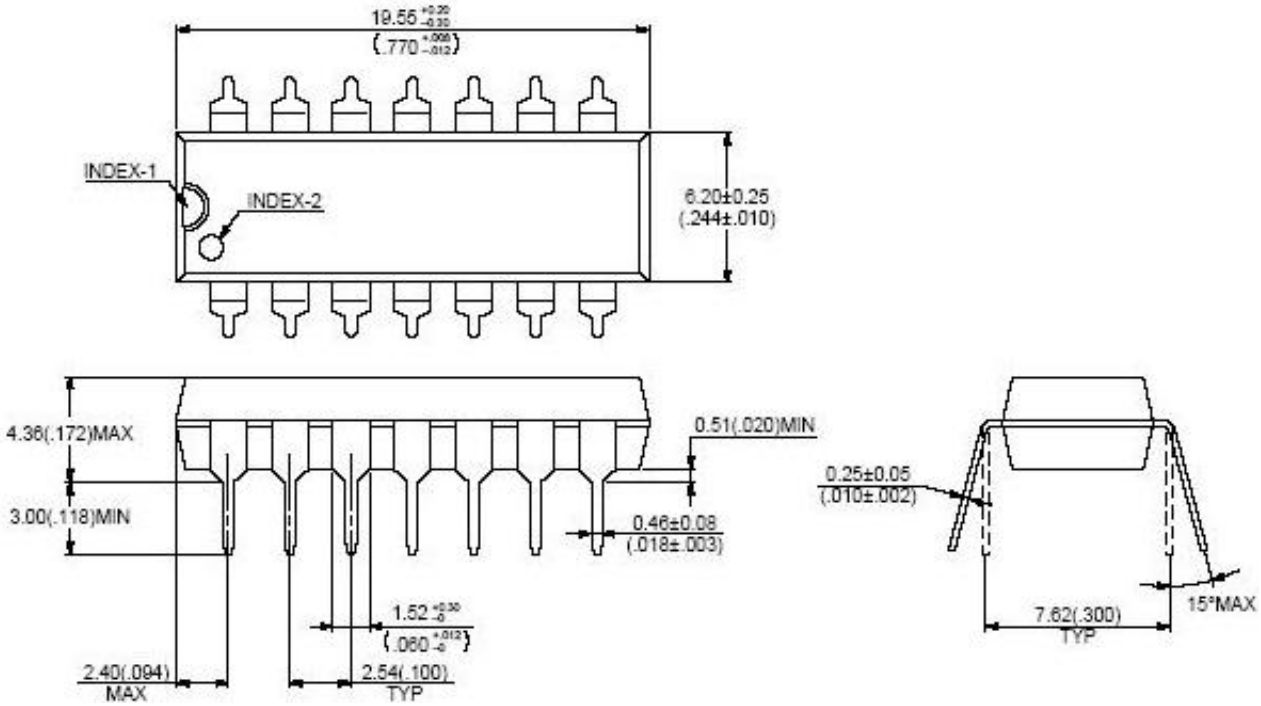
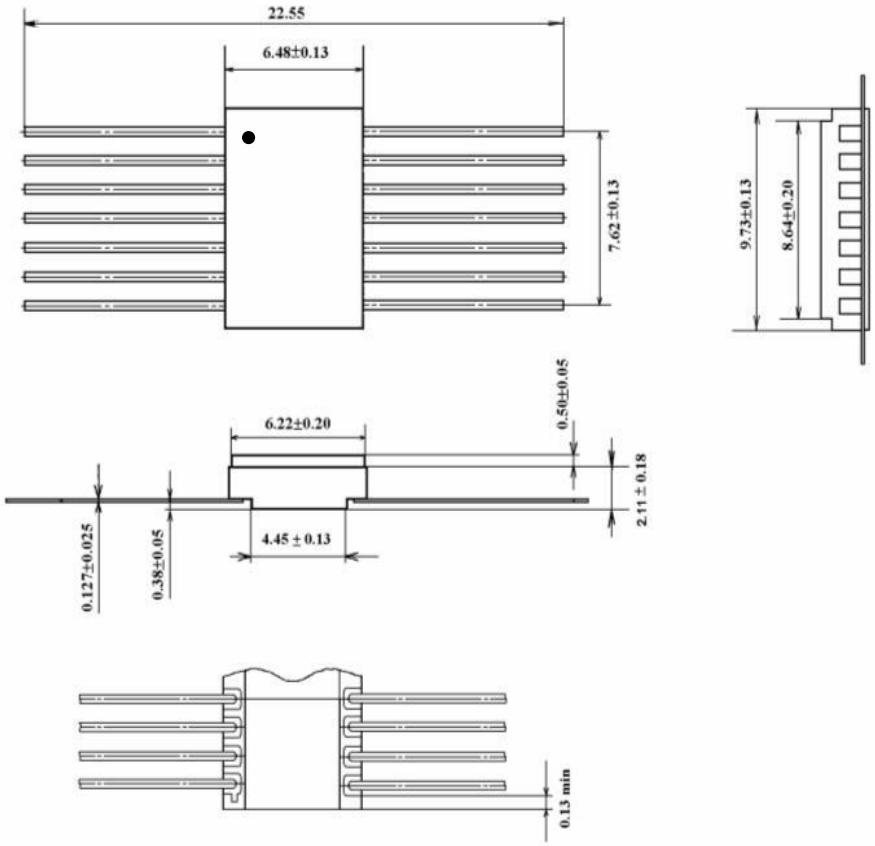


Figure 7

14-LEAD CERAMIC FLATPACK DIMENSIONS



All RD ALFA Microelectronics semiconductor products are manufactured, assembled and tested under ISO9001 quality systems certification.

RD ALFA Microelectronics products are sold by description only. RD ALFA Microelectronics reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by RD ALFA Microelectronics is believed to be accurate and reliable. However, no responsibility is assumed by RD ALFA Microelectronics or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of RD ALFA Microelectronics or its subsidiaries.

For information regarding RD ALFA Microelectronics and its products, see web site http://www.rdalfa.eu