High bandwidth, High Slew Rate, Uncompensated, High Input Impedance, Operational Amplifiers

Operational amplifiers αRD2520 delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

100 V/µs slew rate and 200 ns (0.1 %) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for RF and video circuitry requiring up to 20 MHz gain bandwidth and 2 MHz power bandwidth. For accurate signal conditioning designs the αRD2520's superior dynamic specifications are complemented by 25nA offset current, 50MΩ input impedance and offset trim capability.

These amplifiers have been developed and certified as HiRel and high RadHard components for airspace and defense equipment.

Ordering information

Part	Mark.	Temp., °C	Package	Package drawing
αRD2520/C5B	2520	-60 to +125	8-lead metal can	SH-8
αRD2522/C5B	2522			

Notes:

1. This Pb-free hermetic packaged products employ 100% Au plate, which is RoHS.

Features

- High slew rate. . . . . 100 V/µs
- Fast Settling . . . . . 500 ns
- Full Power Bandwidth. . . . . 2 MHz
- Gain Bandwidth. . . . . 20 MHz
- High Input Impedance. . . . . 50 MΩ
- Low Offset Current. . . . . 25 nA
- High RadHard. . . . . 10^5 rad
- Compensation Pin for Unity Gain Capability
- Balance pins
- RoHS Compliant

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Pinout

8-lead metal can
Top View

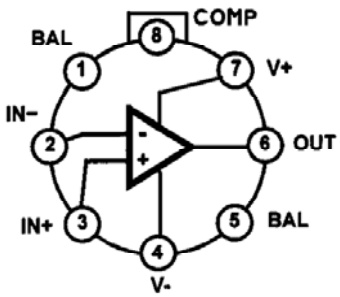


Figure 1. Package pinout

Absolute Maximum Ratings

SupplyVoltage(BetweenV+andV-Terminals)..36 V
Differential Input Voltages. . . . . 10 V
Common Mode Input Voltage (note 3) . . . . . 10 V
OutputCurrent. . . . . 10 mA
Total Power (from -60 °C to 108 °C) . . . . . 350 mW
Total Power (above 108°C) – see fig.20
Short circuit at the output . . . . . 10 s
Notes:

2. While of the same time of above mentioned supply voltage and output current not more 1 h
3. Common mode Input Voltage is determined in accordance with fig.11

Operation Condition

Temperature range -60 °C to +125 °C
Operating Supply Voltage ± 15 V ±10 %
R_L ≥2 kΩ

Thermal Information

Thermal Resistance (typical)
θ_{JA} = 170 °C/W (note 4)
θ_{JC} = 85 °C/W (note 5)
Maximum junction temperature +170 °C
Lead temperature (soldering 3 s) 350 °C
Notes:

4. θ_{JA} is measured with component on an evaluation PC board in free air
5. For θ_{JC} "case temp" location is the center of metal can

Electrical Specifications

V_{SUPPLY} = ± 15 V ± 10 %

Parameter	Temp., °C	αRD2520/C5B			αRD2522/C5B			Units
		Min (note 6)	Typ	Max (note 6)	Min (note 6)	Typ	Max (note 6)	
Input Characteristics								
Offset Voltage (note 8)	25	-	4.0	9	-	4.0	9	mV
	+125	-	5.3	12	-	5.3	12	
	-60	-	5.3	12	-	5.3	12	
Offset Voltage Drift (note 8)	-60 to 25	-	13	30	-	13	50	µV/°C
	25 to +125	-	13	30	-	13	30	
Average bias current (note 8)	25	-	100	225	-	125	300	nA
	+125	-	175	450	-	270	600	
	-60	-	175	450	-	270	600	
Offset Current (note 8)	25	-	14	30	-	22	50	nA
	+125	-	24	60	-	45	100	
	-60	-	24	60	-	45	100	
Offset Current Drift (note 8)	-60 to 25		225	500	-	225	1000	pA/°C
	25 to +125		225	500	-	225	500	
Maximum Common Mode Voltage (note 9)	25	+10	-	-	+10	-	-	V
	+125	+10	-	-	+10	-	-	
	-60	+10	-	-	+10	-	-	
Minimum Common Mode Voltage (note 9)	25	-	-	-10	-	-	-10	V
	+125	-	-	-10	-	-	-10	
	-60	-	-	-10	-	-	-10	
Input Resistance (note 7)	25	-	50	-	-	50	-	MΩ

Parameter	Temp., °C	αRD2520/C5B			αRD2522/C5B			Units
		Min (note 6)	Typ	Max (note 6)	Min (note 6)	Typ	Max (note 6)	
Transfer characteristics								
Large Signal Voltage Gain (note 9, 14)	25	8	11.8	-	7.5	10	-	kV/V
	+125	7	9.1	-	5.5	7.1	-	
	-60	7	9.1	-	5.5	7.1	-	
Common Mode Rejection Ratio (note 8)	25	82	88	-	82	88	-	dB
	+125	80	88	-	80	88	-	
	-60	80	88	-	80	88	-	
Gain Bandwidth (note 7, 15)	25	10	20	-	10	20	-	MHz
Minimum Stable Gain	25	3	-	-	3	-	-	V/V
Output Characteristics								
Maximum Output Voltage (note 9)	25	9.5	12	-	9.5	12	-	V
	+125	9	10.5	-	9.0	10.5	-	
	-60	9	10.5	-	9.0	10.5	-	
Minimum Output Voltage (note 9)	25	-	-12	-9.5	-	-12	-9.5	V
	+125	-	-10.5	-9	-	-10.5	-9	
	-60	-	-10.5	-9	-	-10.5	-9	
Output Current (note 13)	25	10	12.5	-	10	12.4	-	mA
Full Power Bandwidth (note 13, 16)	25	1.5	2.0	-	1.5	2.0	-	MHz
Transient Response								
Rise Time (note 9, 10, 11, 17)	25	-	25	50	-	25	50	ns
Overshoot (note 9, 10, 17)	25	-	10	25	-	10	25	%
Slew rate (note 9, 10, 12, 19)	25	80	100	-	70	100	-	V/µs
Settling Time (note 8, 18)	25	-	200	-	-	200	-	ns
Power Supply Characteristics								
Supply Current	25	-	6.0	7.0	-	6.0	7.0	mA
	+125	-	6.5	7.5	-	6.5	7.5	
	-60	-	6.5	7.5	-	6.5	7.5	
Power Supply Rejection Ratio (note 11)	25	80	90	-	74	90	-	dB
	+125	80	90	-	74	90	-	
	-60	80	90	-	74	90	-	

Notes:

6. Parameters with Max and Min limits are 100 % tested.
7. Parameter is controlled via design or process parameters and is not directly tested at final production. This parameter is lab characterized upon initial design release, or upon design changes. This parameter is guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
8. R_L = 10 kΩ
9. R_L = 2 kΩ
10. C_L = 50 pF
11. V_{OUT} = ±200 mV
12. V_{OUT} = ±5 V
13. V_{OUT} = ±10 V
14. V_{CM} = ±10 V
15. $A_V \geq 10$
16. Full Power Bandwidth guaranteed based on slew rate measurement using FPBW = Slew Rate/$2\pi V_{OUT\ MAX}$
17. See figure 3 and 4
18. See figure 2 and 5
19. See figure 2 and 4

Test Circuits and Waveforms

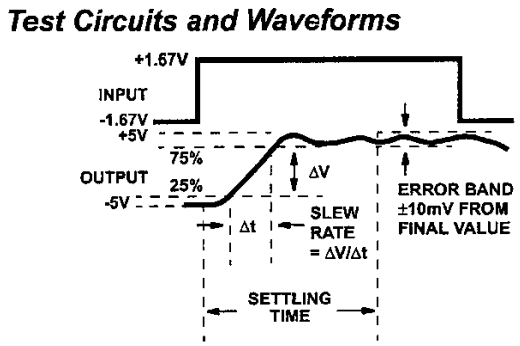


Figure 2. Slew rate and settling time

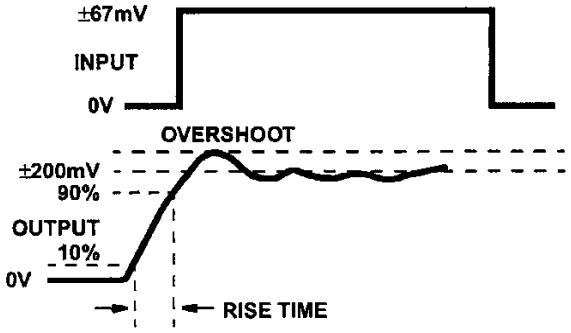


Figure 3.Transient response

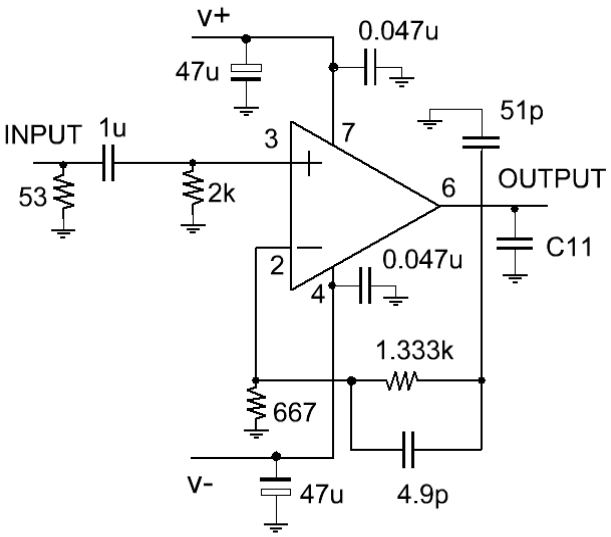


Figure 4. Slew rate and trensient response test circuit

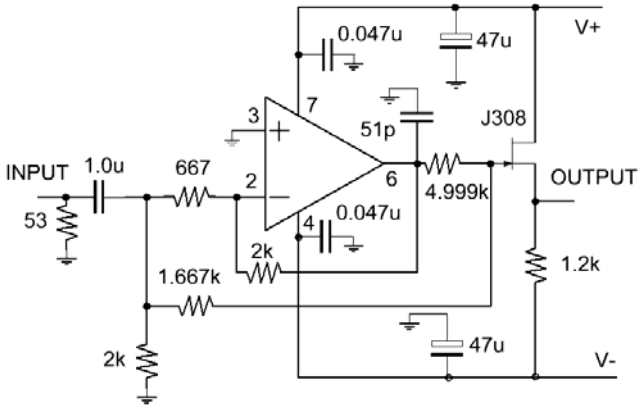


Figure 5. Settling time test circuit

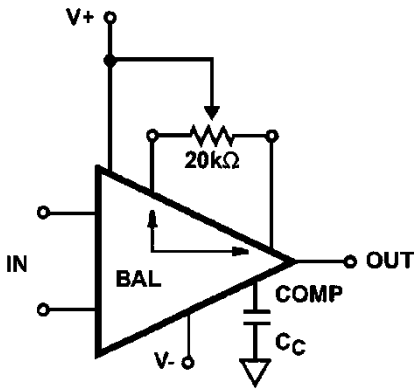


Figure 6. Suggested offset voltage adjustment and compensation hook-up

Schematic Diagram

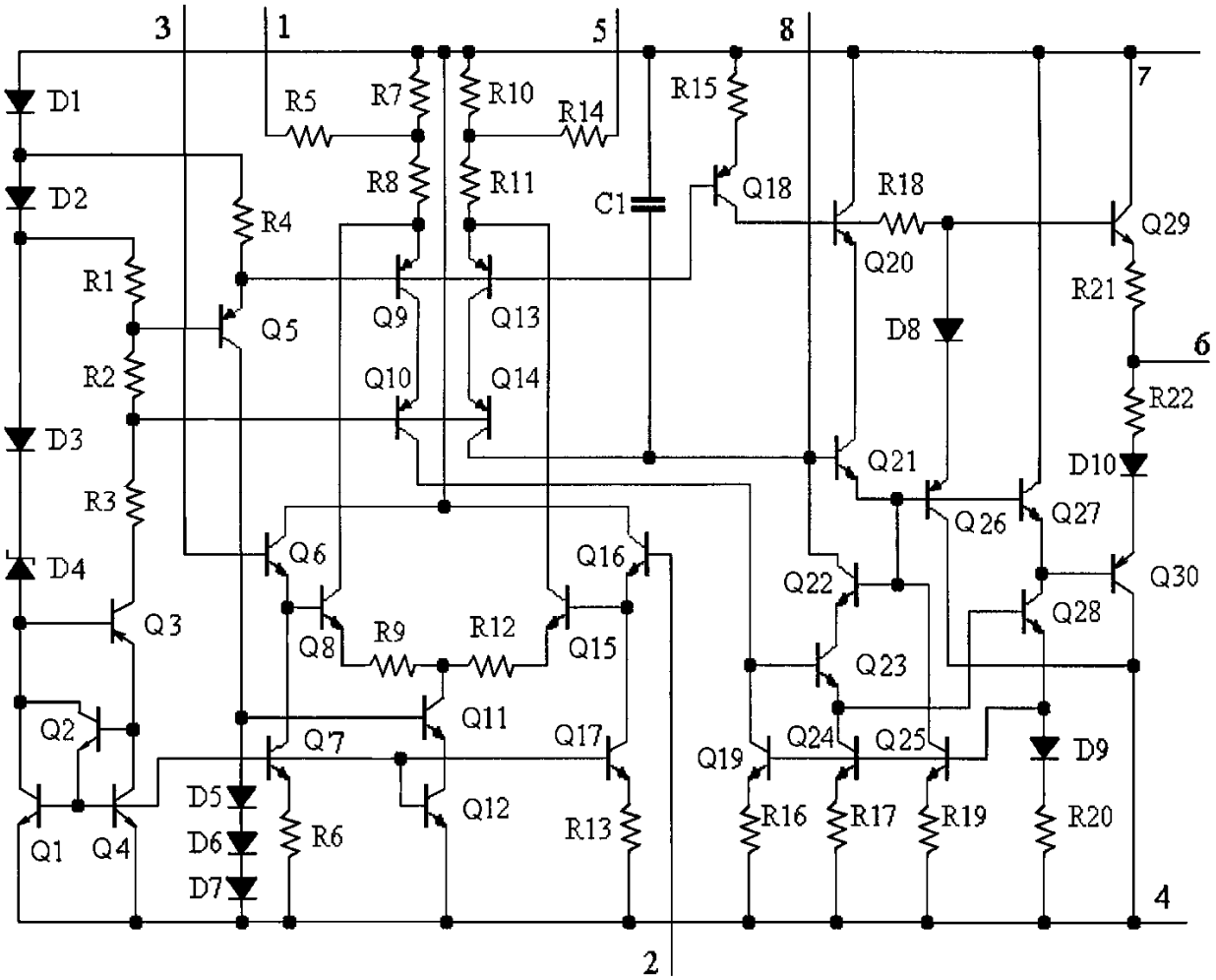


Figure 7.αRD2520,αRD2522 schematic diagram

Typical Application

InvertingUnityGainCircuit

Figure8showsaCompensationCircuitforaninvertingunity gainamplifier.Thecircuitwastestedforfunctionalitywith supplyvoltagesfrom±5 Vto±15V,andtheperformanceas testedwas:SlewRate≈100V/µs;Bandwidth≈7 MHz;and SettlingTime(0.1%)≈500ns.Figure9illustratestheamplifier's frequencyresponse,anditisimportanttonotethatcapacitanc e atpin8mustbeminimizedformaximumbandwidth.

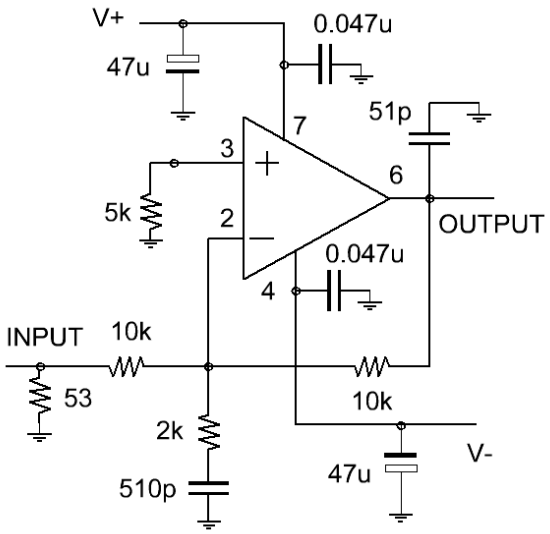


Figure 8.Inverting unity gain circuit

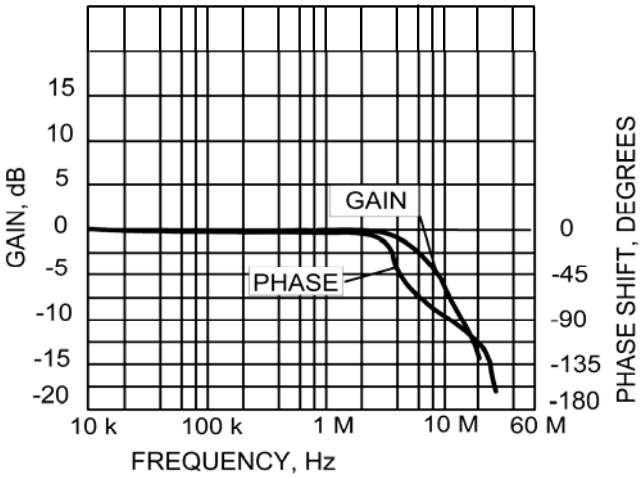


Figure 9. Frequency response for inverting unity gain circuit

Typical Performance Curve

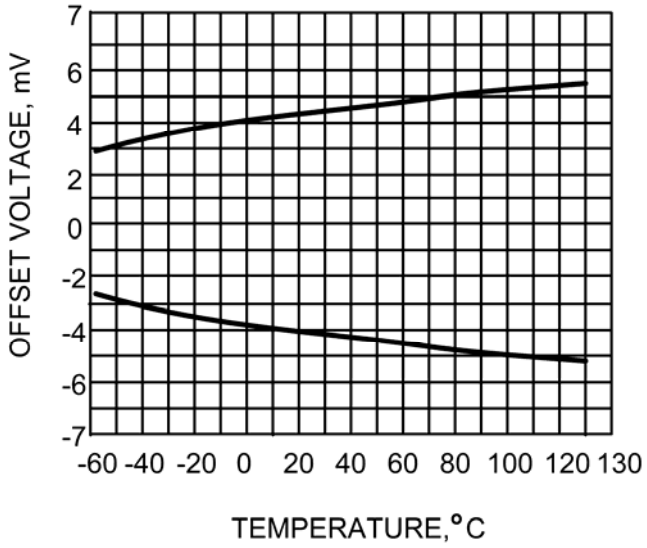


Figure 10. Offset voltage vs temperature

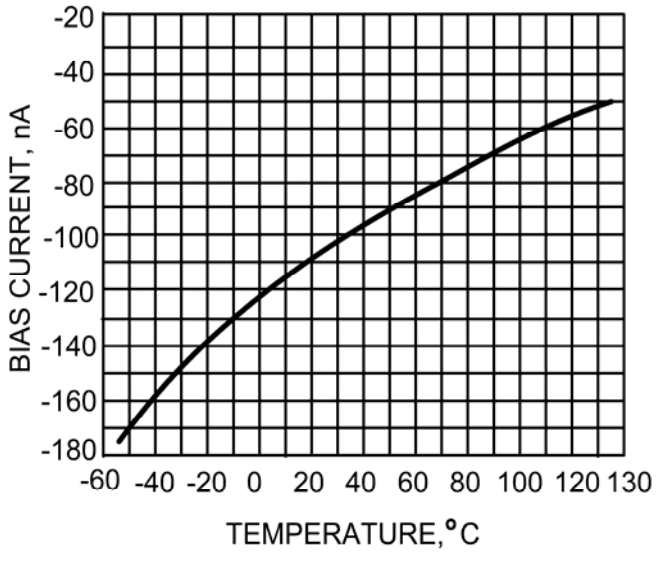


Figure 11. Bias current vs temperature

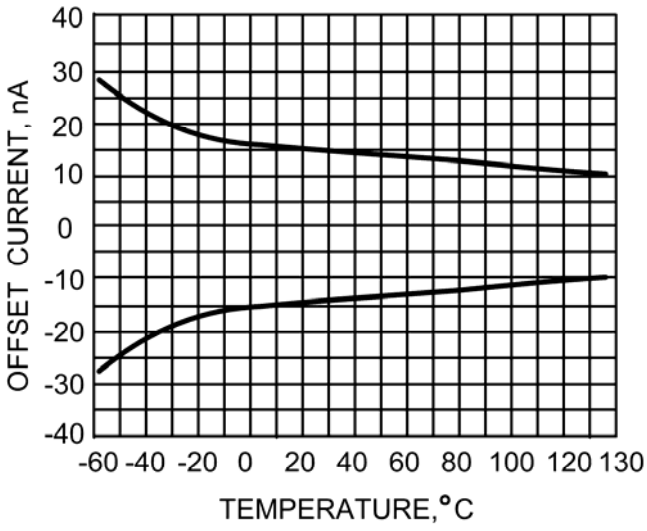


Figure 12. Offset current vs temperature

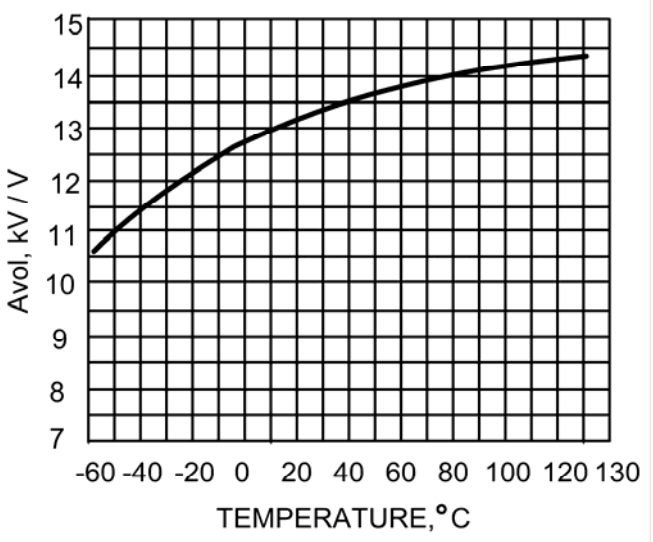


Figure 13. Open loop gain vs temperature

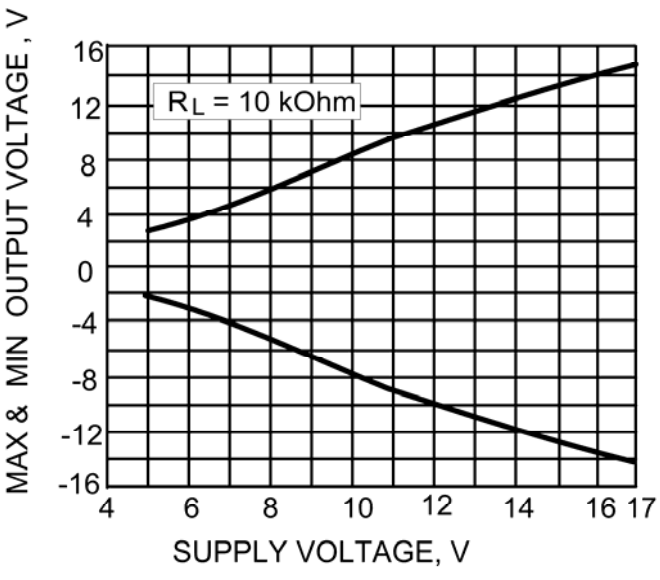


Figure 14. Maximum and minimum output voltage vs supply voltage

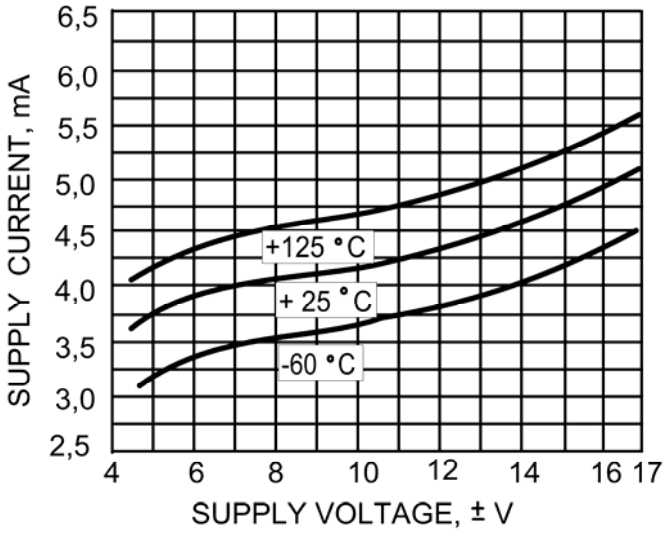


Figure 15. Supply current vs supply voltage

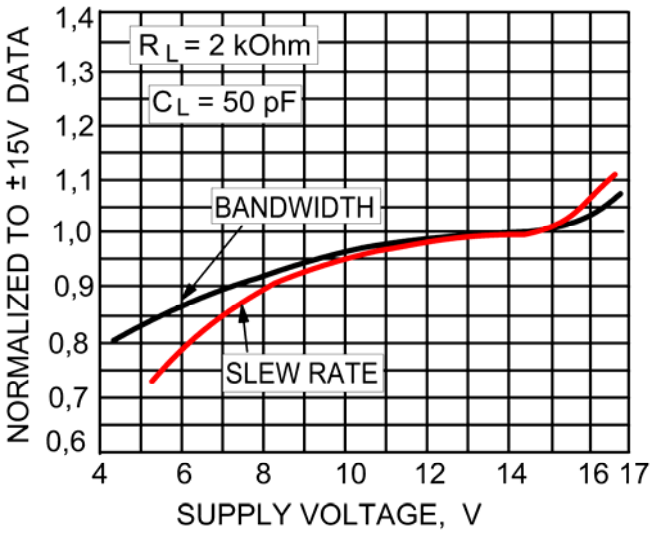


Figure 16. Normalized settling time vs supply voltage

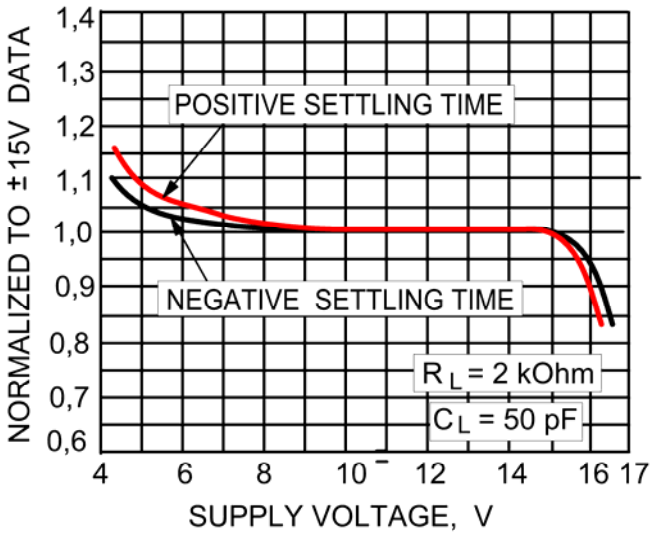


Figure 17. . Normalized slew rate and bandwidth vs supply voltage

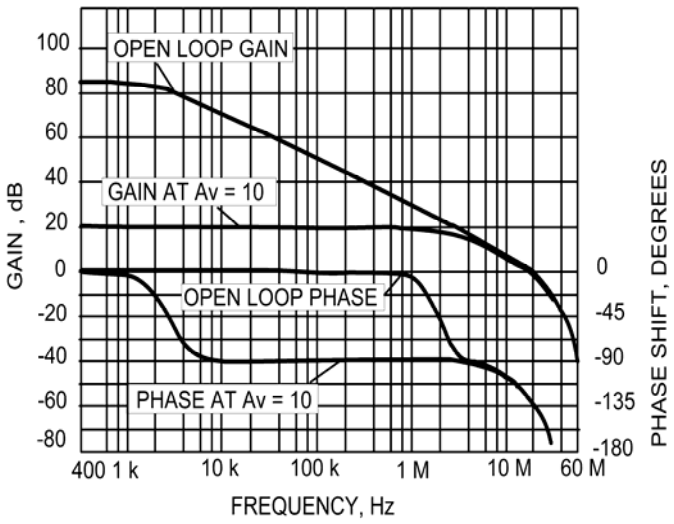


Figure 18. Frequency response

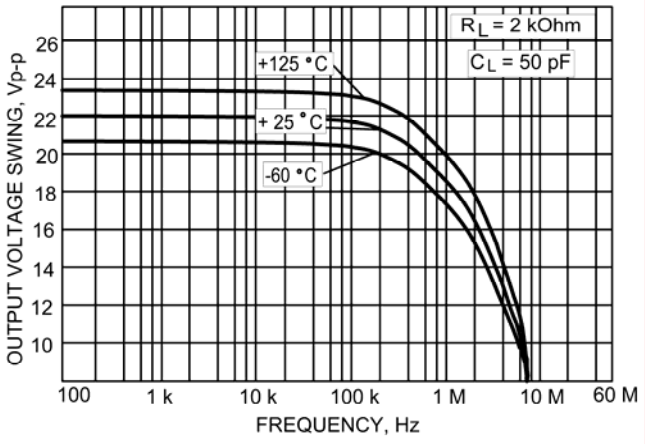


Figure 19. Output voltage swing vs frequency

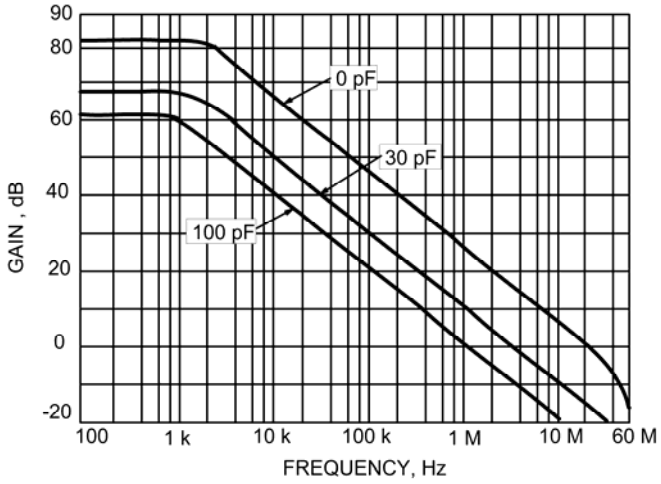


Figure 20. Open loop frequency response for various capacitor values on the comp pin

Die Characteristics

Die dimensions:
1.8x1.7± 0.1 mm,
71x67 ± 4 mils.
Wafer thickness 0.46± 0.02 mm,
18 ± 1 mils.
Metallization:
type: Al, 1% Si,thickness: 1.4 ± 0.1 µm
Glassivation:
type: Phosphosilicate glass (PSG)
PSG thickness 1.2 ±0.2µm.

Worst case current density:
$8 \cdot 10^4$ A/cm^2.
Substrate potential(Powered Up):
Unbiased.
Transistor count:
30.
Process:
Bipolar epitaxial.

Metallization Mask layout

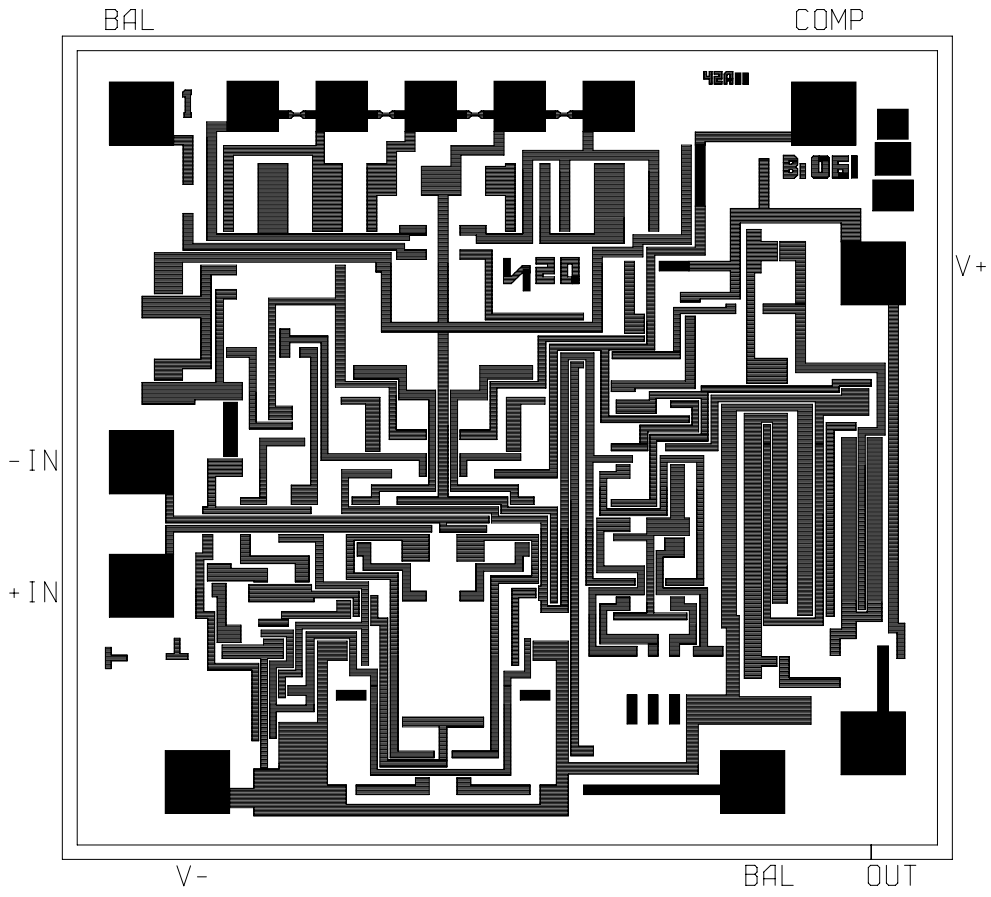
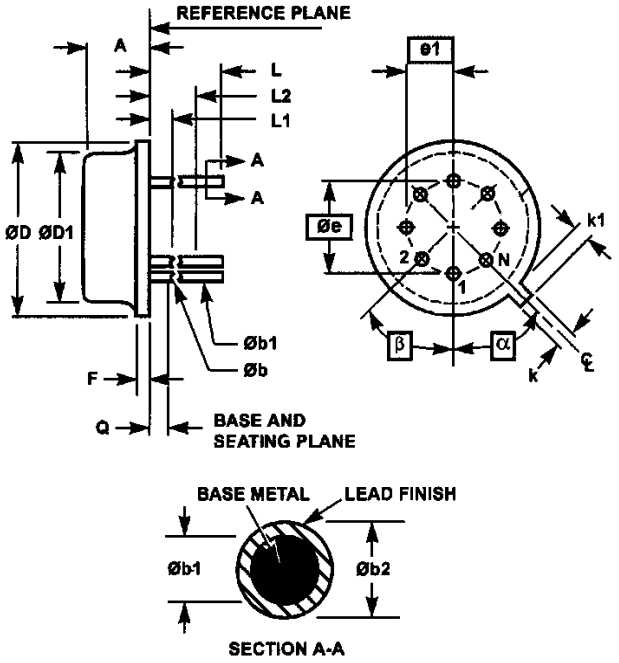


Figure 21.Metallization layout

Metal Can Package



SF-8

8-lead metal can package

Symbol	Millimeters		Inches		Note
	MIN	MAX	MIN	MAX	
A	6.00	6.22	0.236	0.244	-
Øb	0.41	0.48	0.016	0.019	13
Øb1	0.41	0.53	0.016	0.021	13
Øb2	0.41	0.61	0.016	0.024	-
ØD	9.09	9.19	0.335	0.375	-
ØD1	8.23	8.43	0.305	0.335	-
Øe	0.200		5.08		-
e1	0.100		2.54		-
F	0.33	0.43	0.013	0.017	-
k	0.69	0.86	0.027	0.034	-
k1	0.69	1.14	0.027	0.045	14
L	13.0	14.0	0.512	0.552	13
L1	-	1.27	-	0.05	13
L2	6.35	6.85	0.250	0.270	13
Q	0.5	-	0.02	-	-
α	45°		45°		15
β	45°		45°		15
N	8		8		16

Figure 22. Package

Notes:

20. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
21. Measured from maximum diameter of the product.
22. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from a, looking at the bottom of the package.
23. N is the maximum number of terminal positions.
24. Controlling dimension: millimeter.

All RD ALFA Microelectronics semiconductor products are manufactured, assembled and tested under ISO9001 quality systems certification.

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