Quad Operational Amplifiers

αRD148/N5B, αRD148/B5B, αRD148/Z5B, αRD148/Z7B

αRD149/N5B, αRD149/B5B, αRD149/Z5B, αRD149/Z7B

September 28, 2012
RDm037D

General Description

The αRD148/149 is a true quad 741. It consists of four independent, high gains, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the classic 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The αRD149 series has the same features as the αRD148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The αRD148/149 can be used anywhere multiple 741 type amplifiers are being used and in applications where amplifier matching or high packing density is required. These amplifiers have been developed and certified as HiRel and RadHard components for airspace and defense equipment. High reliability is ensured by microcircuit manufacturing process, briefly described in the section "Process Flow" (Figure 1). Radiation tolerance is not less than 100 kRad (Si).

The αRD148/149 is in conformity with Directive 2011/65/EU of 8 June 2011 and don't use hazardous substances.

Features

- 741 op amp operating characteristics
- Class AB output stage—no crossover distortion
- Overload protection for inputs and outputs
- Low supply current drain: 0.6 mA/Amplifier
- Low input offset voltage: 1 mV
- Low input offset current: 4 nA
- Low input bias current 30 nA
- High degree of isolation between amplifiers: 120 dB
- Gain bandwidth product
  αRD148 (AV=1): 1.0 MHz
  αRD149 (AV≥ 5): 4 MHz

Applications

- Data Acquisition Systems
- Analogue Filters
- Instrumentation Amplifiers
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Ordering information

Part	Temp., °C	Package	Package drawing
αRD148/N5B	-60 to +125	14-lead Flat	CSOF-14
αRD149/N5B			
αRD148/B5B		14-lead Dip	CDIP-14
αRD149Z5B			
αRD148/Z5B αRD148/Z7B		20-lead CLCC	CQFN-20
αRD149/Z5B αRD149/Z7B			

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240 Maskavas, Riga 1063, Latvia
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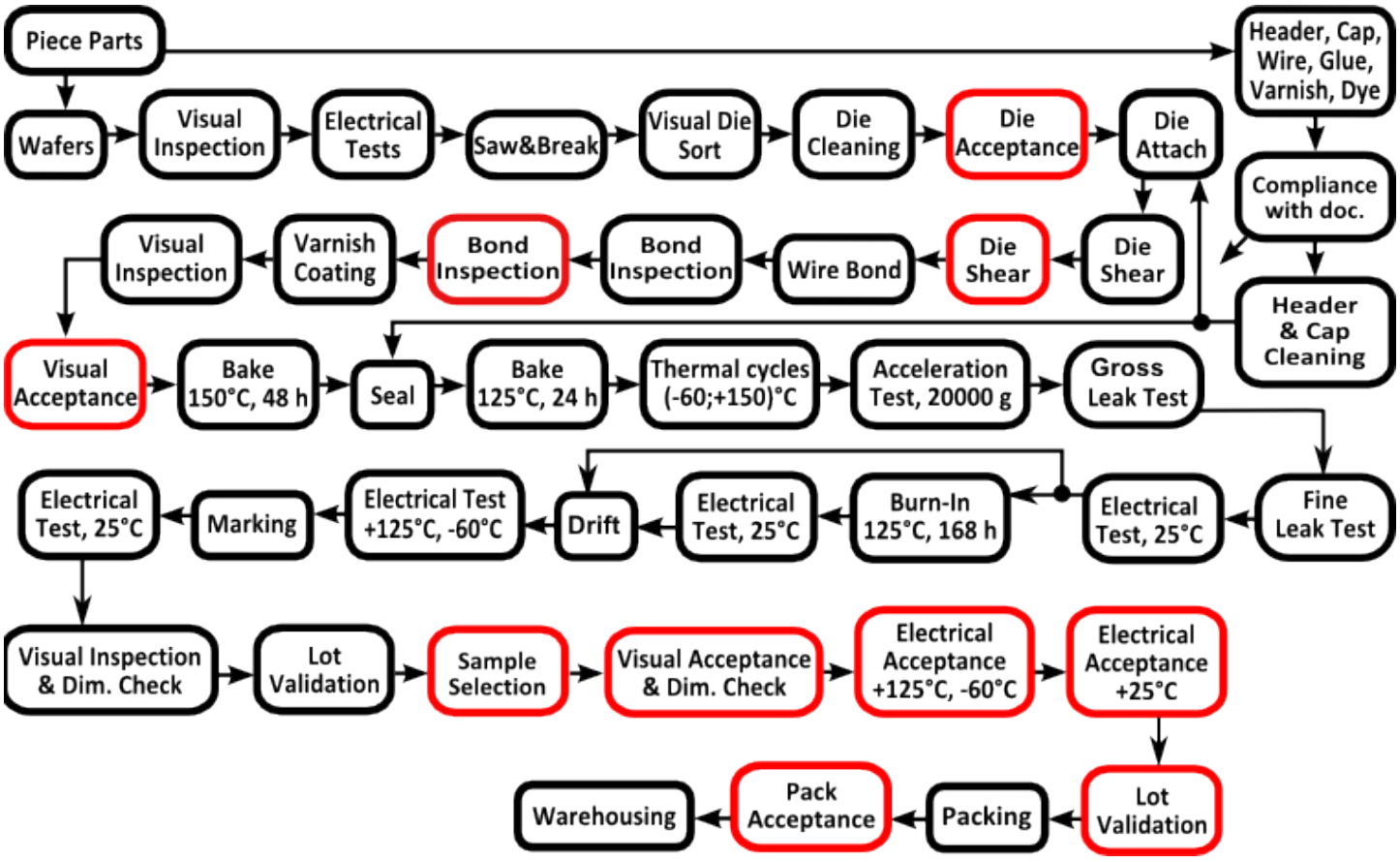
Pin Function Descriptions

Description	Mnemonic	Pin No		
		CSOF-14	CDIP-14	CQFN-20
Output amplifier 1	OUT1	1	1	2
Negative input amplifier 1	-IN1	2	2	3
Positive input amplifier 1	+IN1	3	3	4
Positive supply	V_S+	4	4	6
Positive input amplifier 2	+IN2	5	5	8
Negative input amplifier 2	-IN2	6	6	9
Output amplifier 2	OUT2	7	7	10
Output amplifier 3	OUT3	8	8	12
Negative input amplifier 3	-IN3	9	9	13
Positive input amplifier 3	+IN3	10	10	14
Negative supply	V_S-	11	11	16
Positive input amplifier 4	+IN4	12	12	18
Negative input amplifier 4	-IN4	13	13	19
Output amplifier 4	OUT4	14	14	20

Process Flow

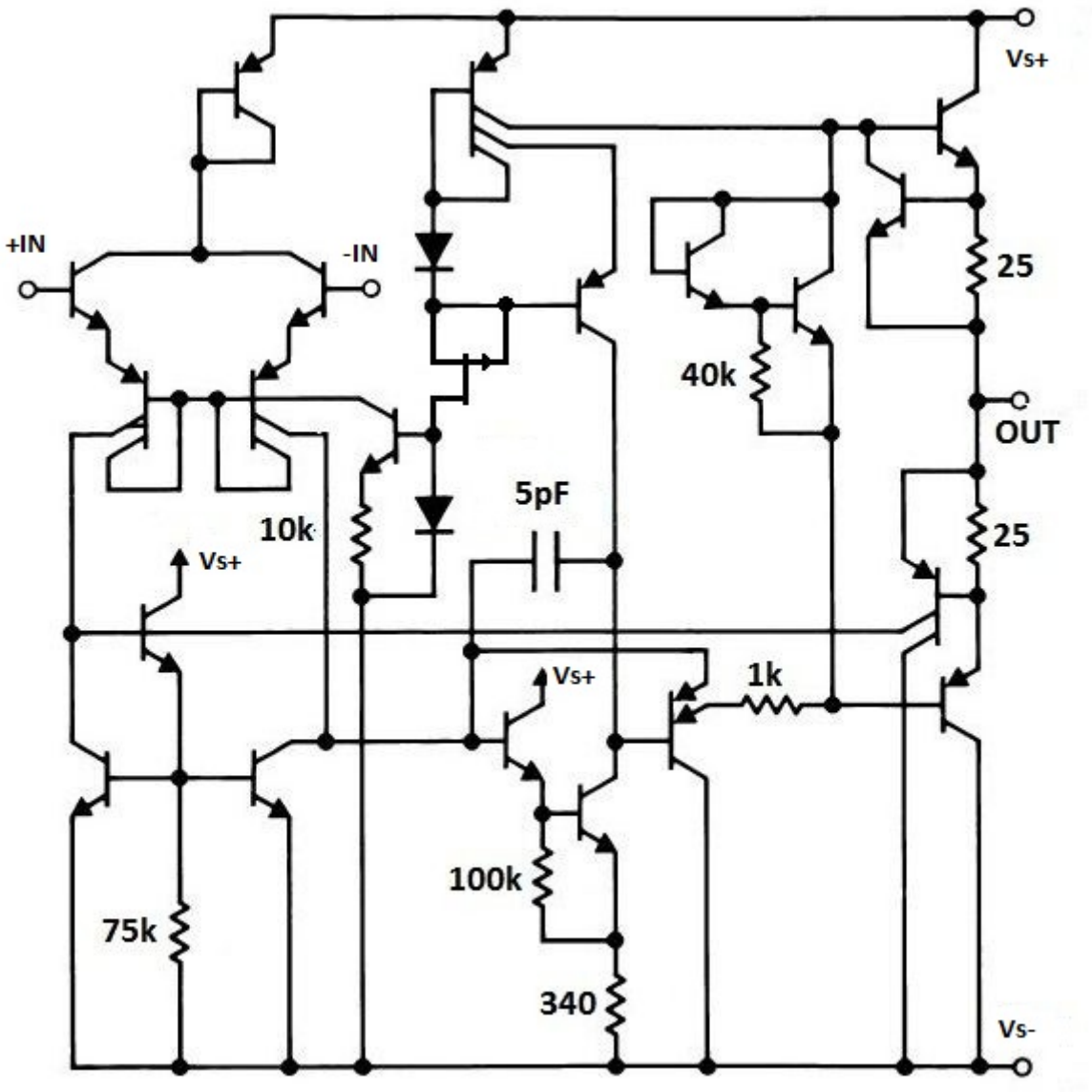


Notes:

1. Color shows the quality assurance procedures

Figure 1. Process Flow

Schematic Diagram



Notes:

2. In the αRD149, 1pF instead of 5 pF

Figure 2. αRD148, αRD 149 Schematic Diagram (1/4 IC)

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals). . .44 V
Differential Input Voltages . . . . . 30 V
Common Mode Input Voltage . . . . . .15 V
Output Current . . . . . 25 mA
Total Power (note 3) . . . . . .1 W
Output Short Circuit Duration (note 4) . . . .Continuous

Thermal Information

Thermal Resistance (typical)(note 6)
θ_{JA} = 25 °C/W (CDIP-14)
θ_{JA} = 60 °C/W (CSOF-14)
Maximum Junction Temperature +175 °C
Lead Temperature (soldering 3 s) 350 °C

Operation Condition

Operating Temperature Range -60 °C to +125 °C
Storage Temperature Range −65 ˚C to +150 ˚C
Operating Supply Voltage ± 15 V ±10 %
Allowable load $R_L \geq 2$ kΩ
ESD Tolerance (note 5) 500 V

Notes:

3. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less.
4. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
5. Human body model, 1.5 kΩ in series with 100 pF.
6. θ_{JA} is measured with component on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ± 15 V ± 1 % (unless otherwise specified)

Parameter	Temp., °C	αRD148		αRD149		Unit
		Min	Max	Min	Max	
Input Characteristics						
Input Offset Voltage	25	-5	+5	-5	+5	mV
	+125	-6	+6	-6	+6	
	-60	-6	+6	-6	+6	
Input Offset Voltage Drift (note 7)	-60 to +25	-	0.2	-	0.2	µV/°C
	+25 to +125	-	0.1	-	0.1	
Input Bias Current	25	1	100	1	100	nA
	+125	1	100	1	100	
	-60	1	325	1	325	
Input Offset Current	25	-25	+25	-25	+25	nA
	+125	-25	+25	-25	+25	
	-60	-75	+75	-75	+75	
Input Offset Current Drift (note 7)	-60 to +25	-	0.25	-	0.25	nA/°C
	+25 to +125	-	0.25	-	0.25	
Noise						
Broadband Noise (note 15)	25	-	15	-	15	μV_{RMS}
Popcorn Noise	25	-	40	-	40	μV_{PK}

Parameter	Temp., °C	αRD148		αRD149		Unit
		Min	Max	Min	Max	
Output Characteristics						
Maximum Output Voltage (note 8)	25	9.5	-	9.5		V
	+125	9.0	-	9.0		
	-60	9.0	-	9.0		
Minimum Output Voltage (note 8)	25	-	-9.5	-	-9.5	V
	+125	-	-9.0	-	-9.0	
	-60	-	-9.0	-	-9.0	
Source and Drain Short Circuit Current	25	-55	-14	-55	-14	mA
Transfer Characteristics						
Large Signal Voltage Gain (note 8, 11)	25	50	-	50	-	V/mV
	+125	25	-	25	-	
	-60	25	-	25	-	
Common Mode Rejection Ratio (note 12)	25	70	-	70	-	dB
	+125	70	-	70	-	
	-60	70	-	70	-	
Power Supply Rejection Ratio (note 13)	25	77	-	77	-	dB
	+125	77	-	77	-	
	-60	77	-	77	-	
Channel Separation (note 11, 14)	25	80	-	80	-	dB
Dynamic Characteristics						
Slew rate (note 10, 16)	25	0.2	-	2	-	V/µs
Gain Bandwidth Product (note 8)	25	0.4	-	3.4	-	MHz
Power Supply						
Supply Current (note 17)	25	-	4.6	-	4.6	mA
	+125	-	4.6	-	4.6	
	-60	-	5.5	-	5.5	
Drift (αRD148XR7U and αRD149XR7U only) (note 18)						
Input Offset Voltage	25	-1	1	-1	1	mV
Input Bias Current	25	-15	15	-15	15	nA

Notes:

7. Calculated parameter
8. R_L = 2 kΩ
9. V_{OUT} = ±200 mV
10. V_{OUT} = ±5 V
11. V_{OUT} = ±10 V
12. V_{CM} = ±12 V
13. ±5 V ≤V_{SUPPLY}≤±15 V
14. In any combination, 20 Hz to 20 kHz
15. 10 Hz to 5 kHz
16. 148: A_V=1, 149: A_V=5
17. All amplifier
18. Measure each amplifier

Die Characteristics

Die dimensions: 2.1x1.8 ± 0.1 mm.
Wafer thickness: 0.46 ± 0.02 mm.
Metallization: Al, 1% Si, thickness: 1.4 ± 0.1 µm.
Glassivation: phosphosilicate glass (PSG), thickness 1.2 ± 0.2 µm.

Worst case current density: 800 A/mm^2.
Substrate potential: Unbiased.
Transistor count: 94.
Process: bipolar epitaxial.

Metallization Mask Layout

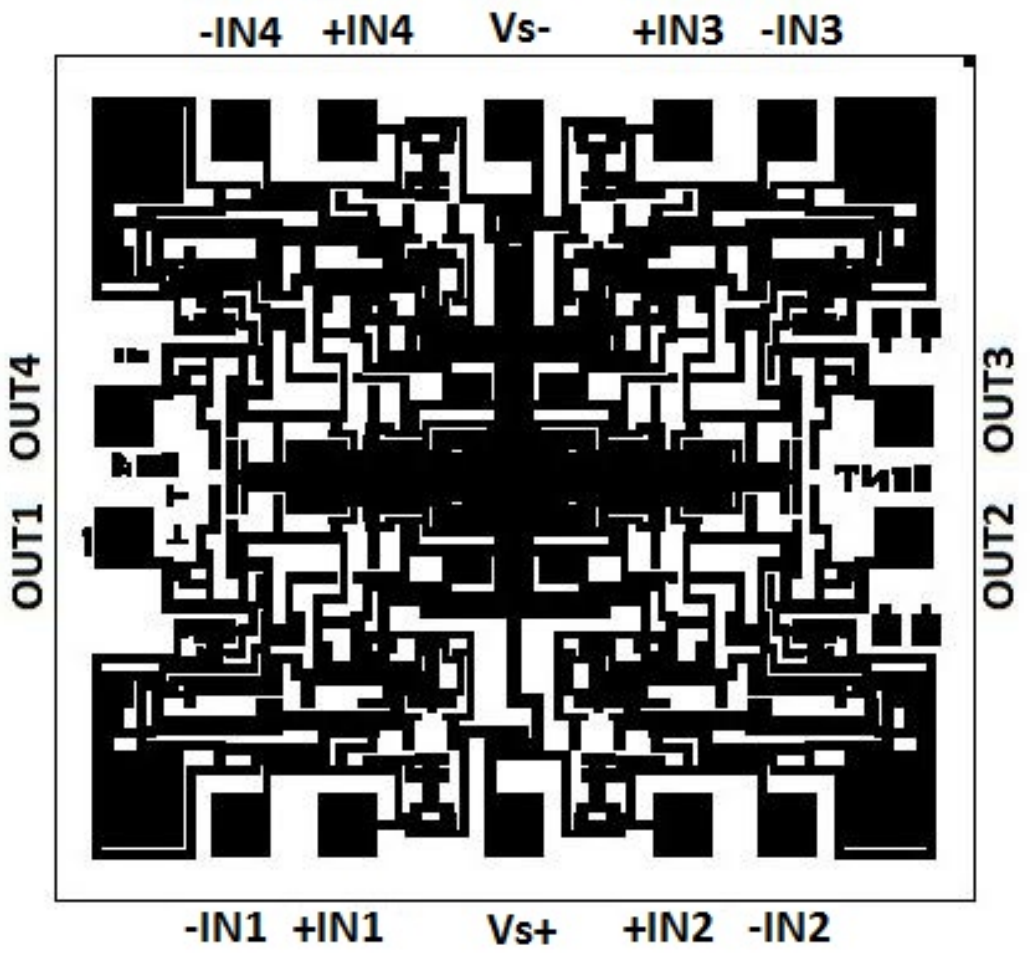


Figure 3. **Metallization mask and pin-outs**

Typical Performance Characteristics

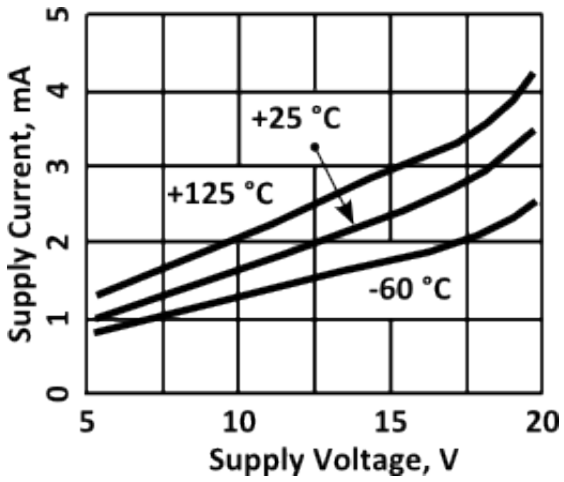


Figure 5. Supply Current vs Supply Voltage

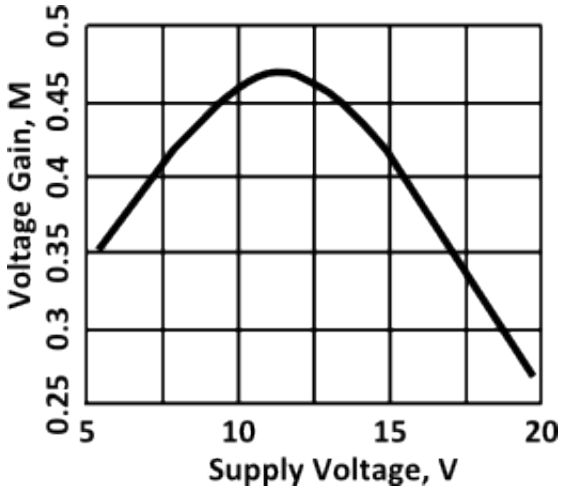


Figure 6. Open Loop Voltage Gain vs Supply Voltage

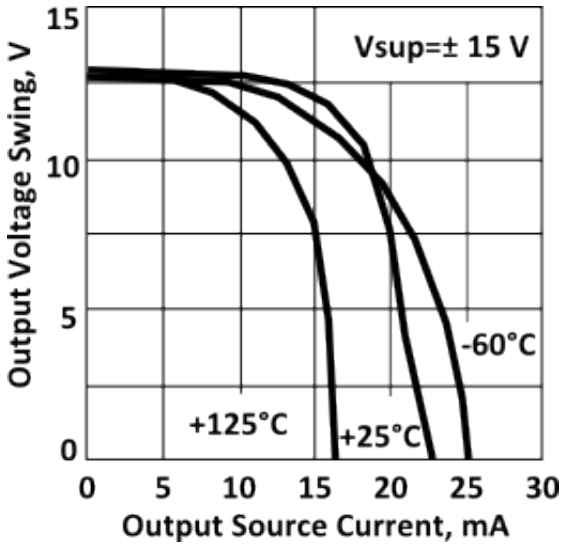


Figure 7. Output Voltage vs Output Source Current

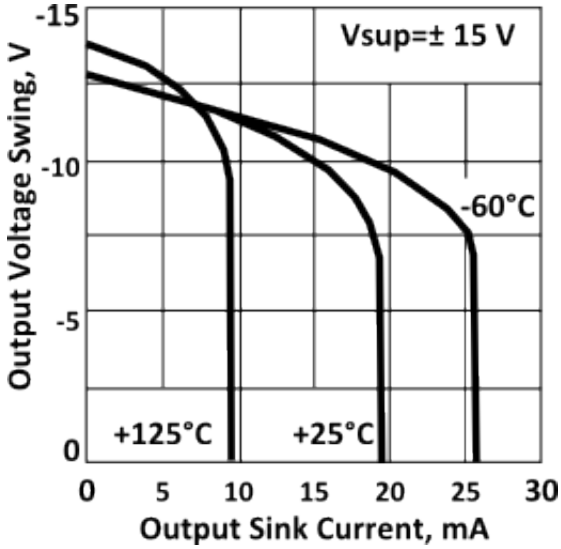


Figure 8. Output Voltage vs Output Source Current

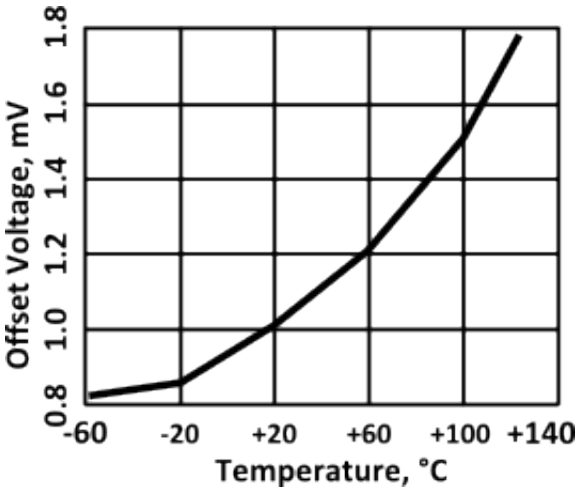


Figure 9. Offset Voltage vs Temperature

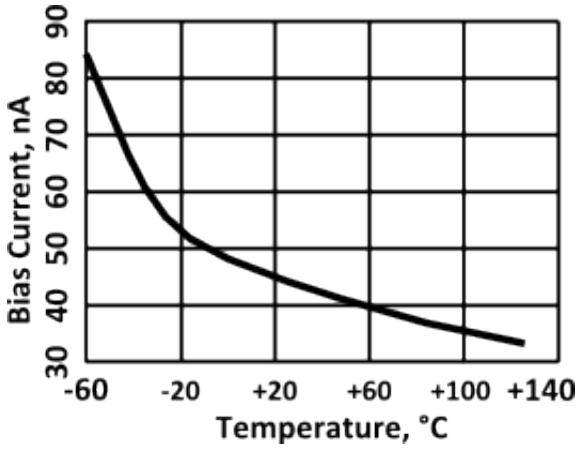


Figure 10. Input Bias Current vs Temperature

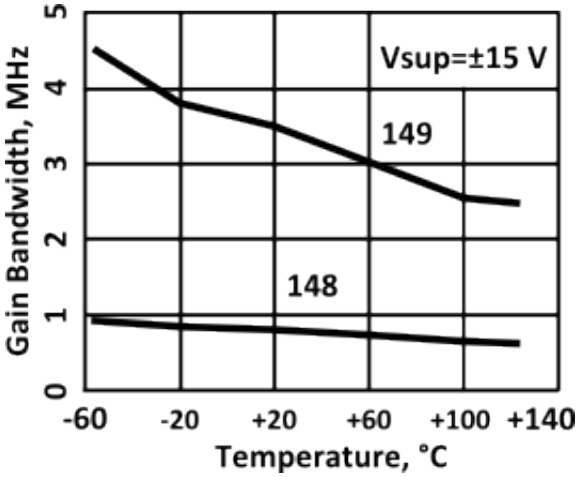


Figure 11. Cain Bandwidth vs Temperature

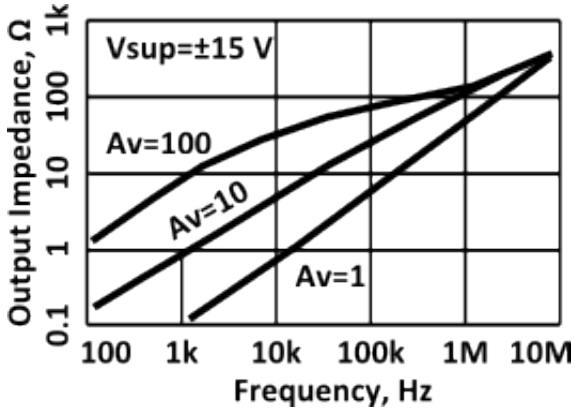


Figure 12. Output Impedance vs Frequency

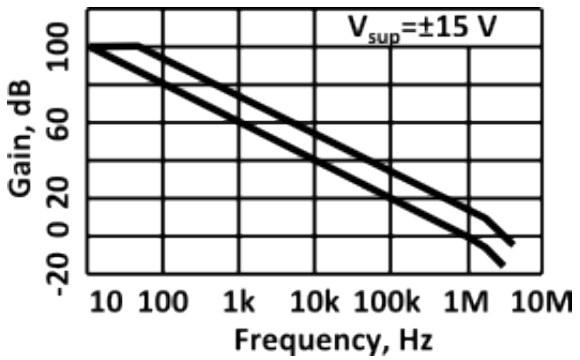


Figure 13. Open Loop Frequency Response

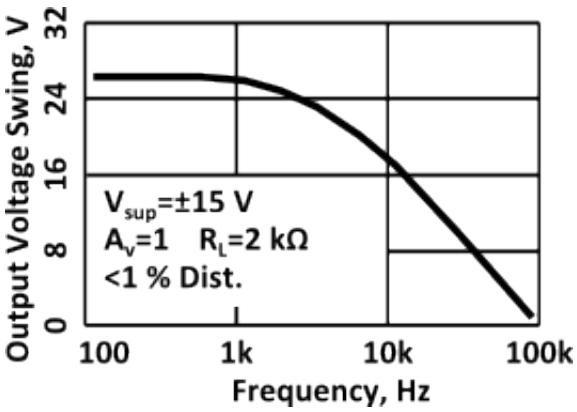


Figure 14. Undistorted Output Voltage Swing vs Frequency

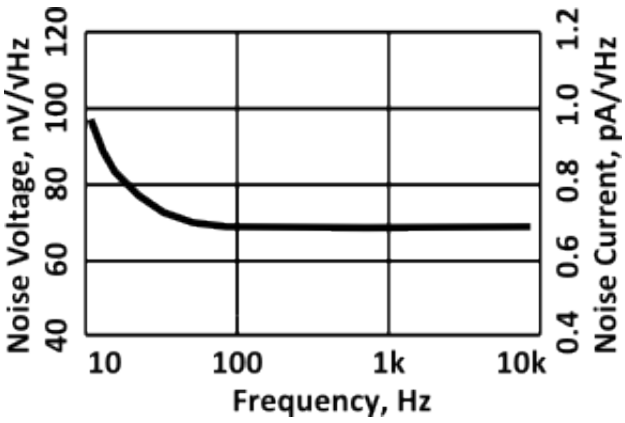


Figure 15. Noise Voltage & Current vs Frequency

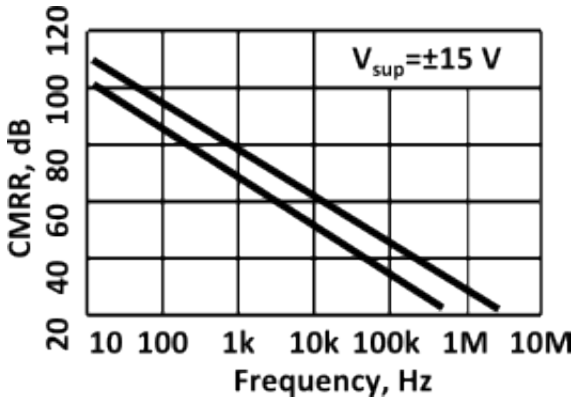


Figure 16. Common Mode Rejection Ratio vs Frequency

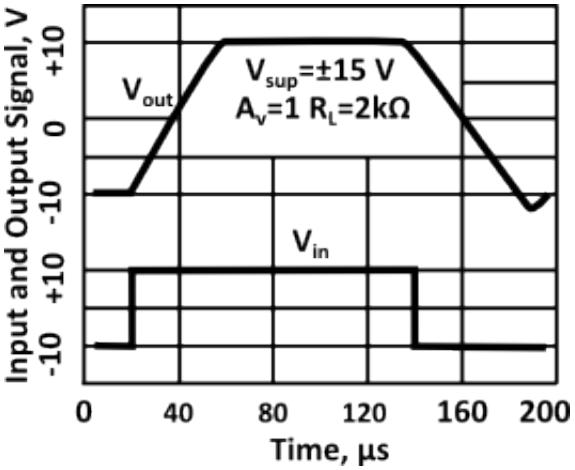


Figure 17. Large Signal Pulse Response (148)

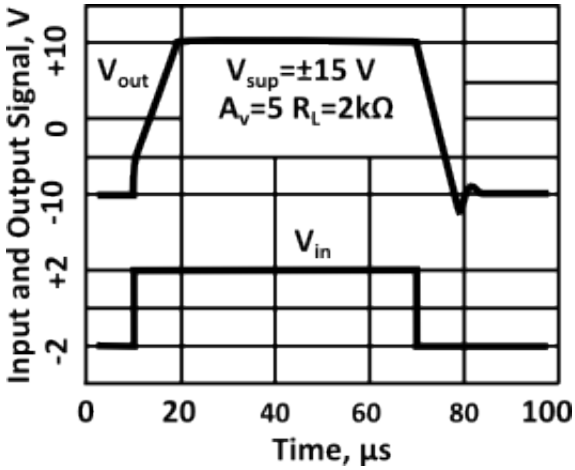


Figure 18. Large Signal Pulse Response (149)

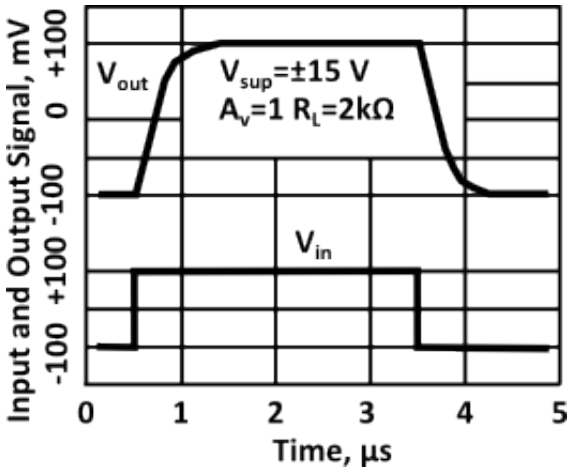


Figure 19. Small Signal Pulse Response (148)

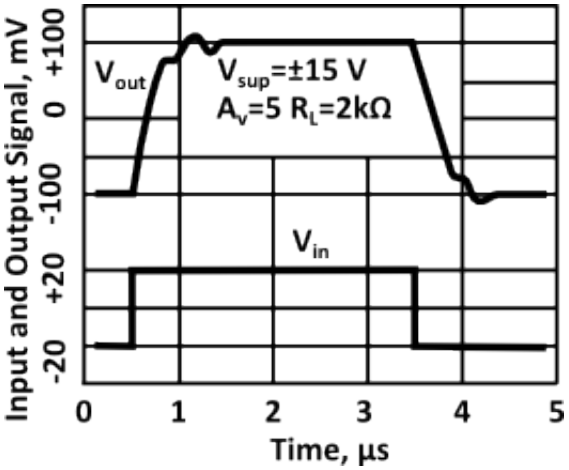


Figure 20. Small Signal Pulse Response (149)

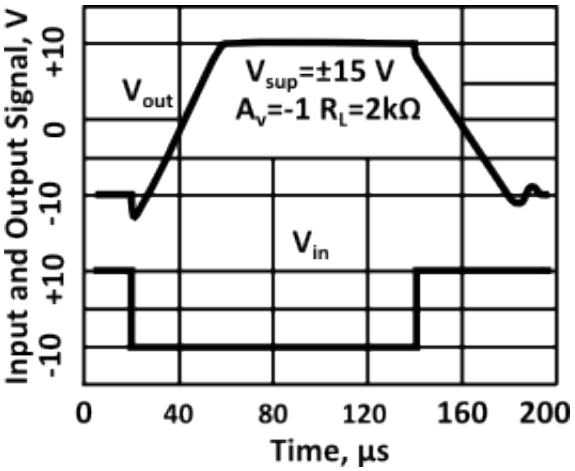


Figure 21. Inverting Large Signal Pulse Response (148)

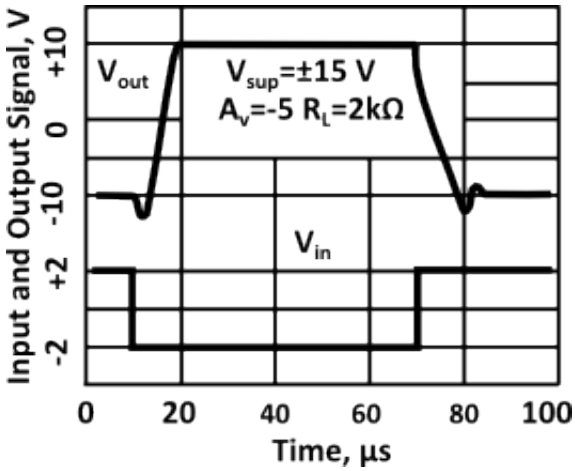


Figure 22. Inverting Large Signal Pulse Response (149)

Application Hints

The αRD148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the αRD148 series op amps can be employed directly with no change in circuit performance. The αRD149 series has the same characteristics as the αRD148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5. The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

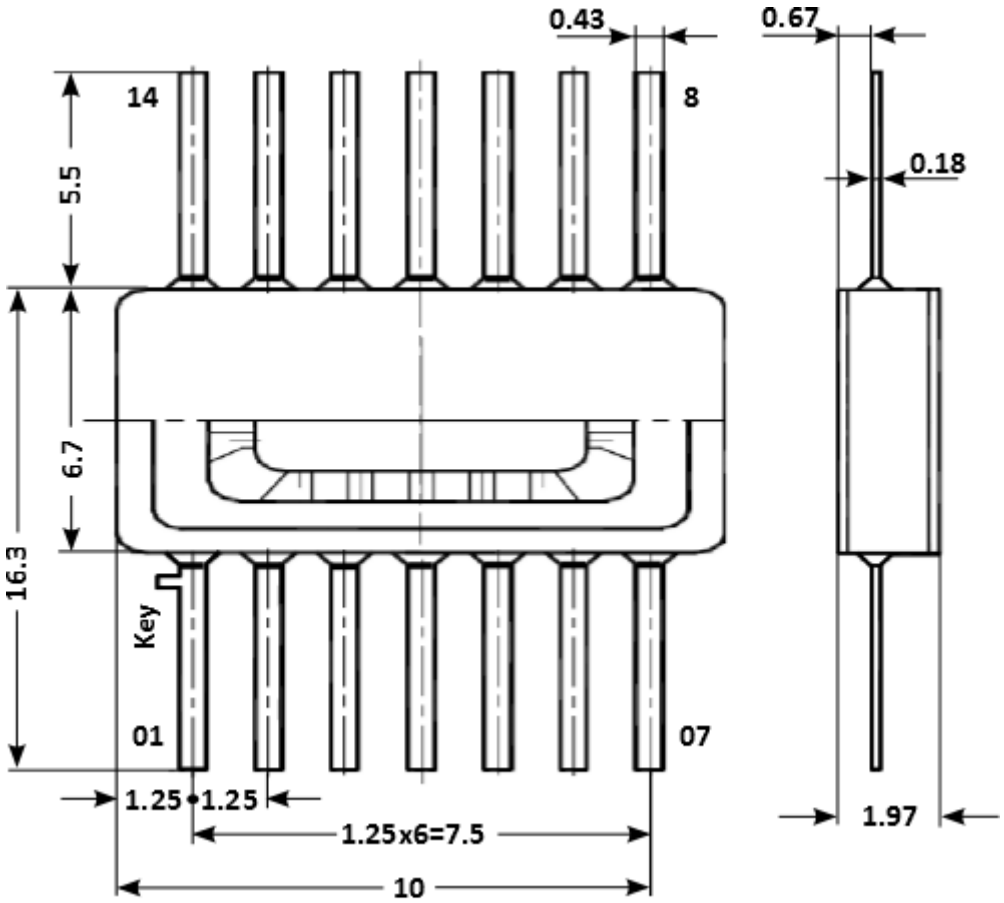
The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current. Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip. As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Physical Dimensions

Flatpack CSOF-14/6.7x10-1.25

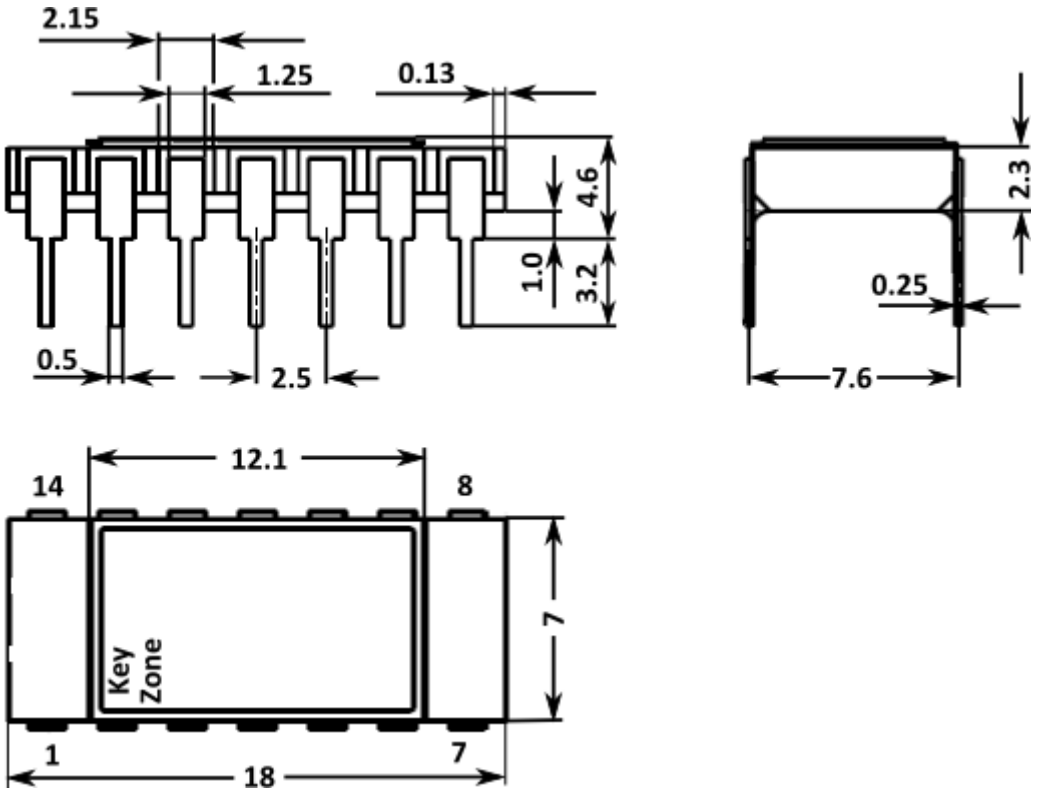


Notes:

19. Lead finish to be 1.0 µm minimum gold over 1.5 µm to 8 µm nickel underplate
20. Lead resistance to be 300 mΩ max

Figure 23. **Ceramic Flat Package**

Cerdip CDIP-14/7x18-2.5

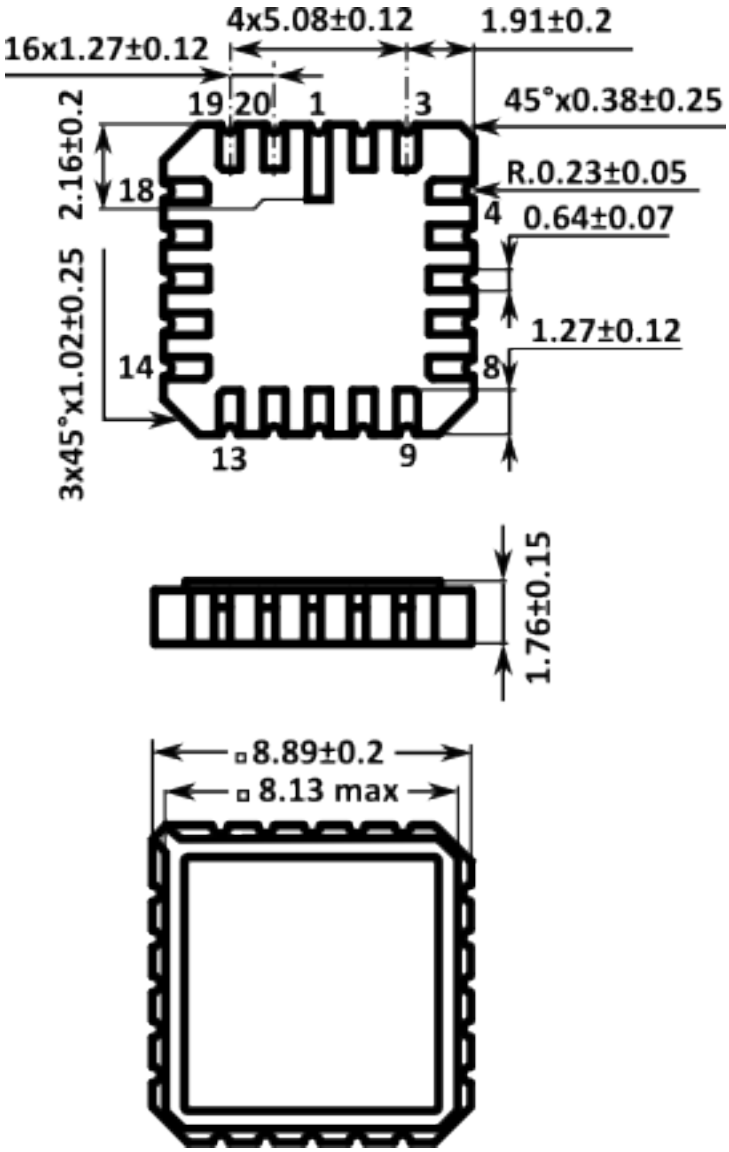


Notes:

21. Lead finish to be 1.5 µm minimum gold over 1.5 µm to 8 µm nickel underplate
22. Dimension 0.13 µm shall be measured from the edge of the furthest extension of the metal pad or lead
23. Lead resistance to be 200 mΩ max

Figure 24. Ceramic DIP Package

Ceramic Leadless Chip Carrier CQFN-20/8.9x8.9-1.27



Notes:

24. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features(e.g., lid, castellations, terminals, thermal pads, etc.)

Figure 25. Leadless Package

Revision History

Date	Release	Used Documents	Changes	Originator
09/28/12	A	JEDEC JESD30E	Writing improvement, typos correction. Addition: package CQFN-20, parts αRD148XR7U, αRD149XR7U	S.Sudin
04/29/12	0	АЕЯР.431130.488 ТУ ОСТ 11 0694-89 RDm037 э3 RDm1002 Д	Original	S.Sudin

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